Dual 3A Low Quiescent Current High Efficiency Synchronous Buck Regulator

ISL8033, ISL8033A

ISL8033 is a dual integrated power controller rated for 3A per channel with a 1MHz step-down regulator that is ideal for any low power low-voltage applications. The ISL8033A offers 2.5MHz operation for smaller more compacted design. The channels are 180° out-of-phase for input RMS current and EMI reduction. It is optimized for generating low output voltages down to 0.8V each. The supply voltage range is from 2.85V to 6V, allowing for the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has a guaranteed minimum output current of 3A each when ISET is connected to VDD. The output current of each output is selectable by setting ISET pin.

The ISL8033, ISL8033A includes a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. 100% duty-cycle operation allows less than 250mV dropout voltage at 3A.

The ISL8033, ISL8033A offers an independent 1ms Power-Good (PG) timer at power-up. When shutdown, ISL8033, ISL8033A discharges the output capacitor. Other features include internal digital soft-start, enable for power sequence, controllable soft-stop output discharge during disabled, start-up with pre-biased output, 100% maximum duty cycle for lowest dropout, 100% duty cycle operation for smooth transition, less than 8µA logic controlled shutdown current, independent enable, overcurrent protection, and thermal shutdown.

The ISL8033, ISL8033A is offered in a 24 Ld 4mmx4mm QFN package with 1mm maximum height. The complete converter occupies less than 5.46cm^2 area.

Features

- Dual 3A High Efficiency Synchronous Buck Regulator with up to 95% Efficiency
- 2% Output Accuracy Over-Temperature/Load/Line
- Internal Digital Soft-Start - 1.5ms
- External Synchronization up to 6MHz (ISL8033)
- Internal Current Mode Compensation
- Peak Current Limiting and Hiccup Mode Short Circuit Protection
- Adjustable Peak Overload Current
- Negative Current Protection
- Pb-Free (RoHS Compliant)

Applications

- DC/DC POL Modules
- µC/µP, FPGA and DSP Power
- Plug-in DC/DC Modules for Routers and Switchers
- Test and Measurement Systems
- Li-ion Battery Power Devices
- Bar Code Readers

Related Literature

- See AN1606, ISL8033EVAL1Z Application Note
- See AN1611, ISL8033EVAL2Z Application Note

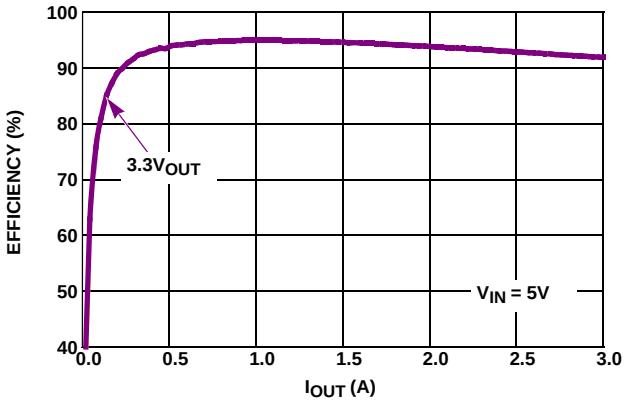


FIGURE 1. EFFICIENCY vs LOAD

Typical Application Circuit

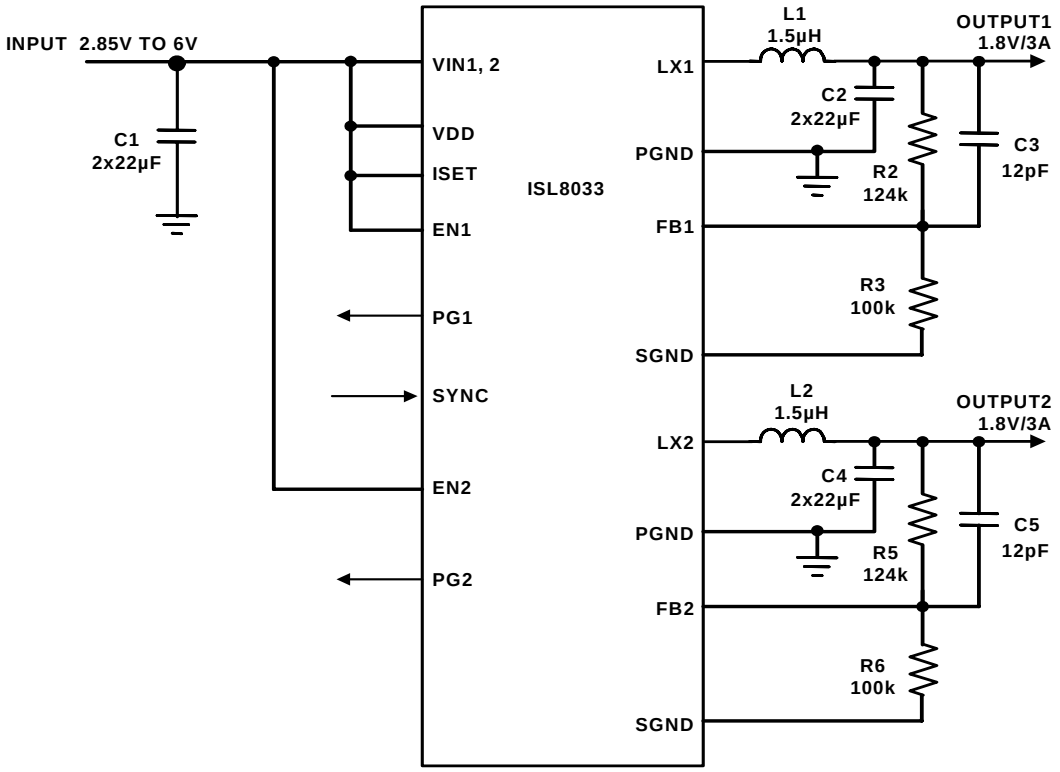


FIGURE 2. TYPICAL APPLICATION DIAGRAM - DUAL INDEPENDENT OUTPUTS

TABLE 1. ISL8033 COMPONENT VALUE SELECTION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2 (or C4)	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C3 (or C5)	12pF	12pF	12pF	12pF	12pF	12pF
L1 (or L2)	1.0µH~2.2µH	1.0µH~2.2µH	1.0µH~2.2µH	1.0µH~3.3µH	1.0µH~3.3µH	1.0µH~4.7µH
R2 (or R5)	0	50k	87.5k	124k	212.5k	312.5k
R3 (or R6)	100k	100k	100k	100k	100k	100k

TABLE 2. ISL8033A COMPONENT VALUE SELECTION

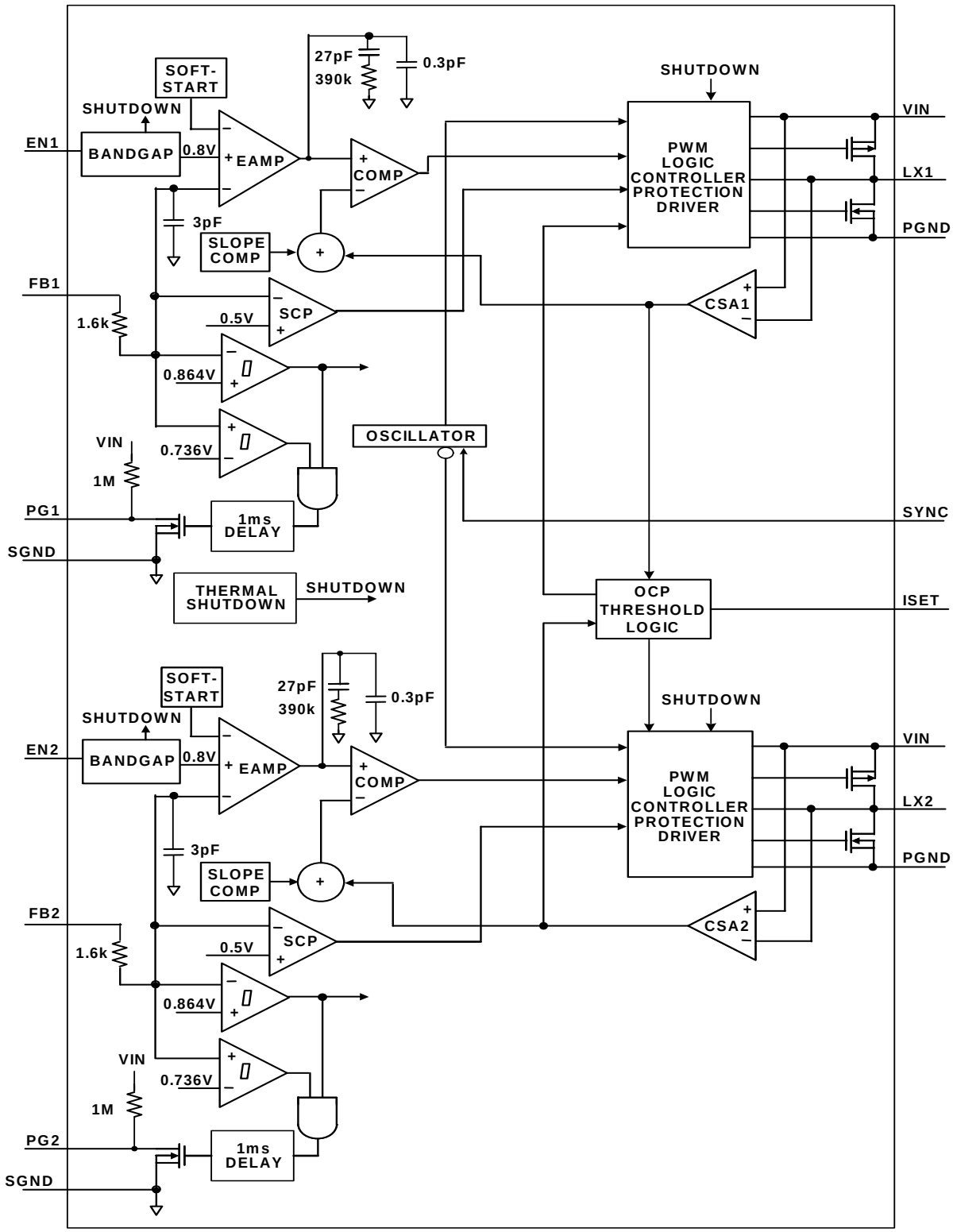
V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
C1	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C2 (or C4)	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF	2x22µF
C3 (or C5)	12pF	12pF	12pF	12pF	12pF	12pF
L1 (or L2)	0.47~1.5µH	0.47~1.5µH	0.47~1.5µH	0.47~1.5µH	1.0~2.2µH	1.0~3.3µH
R2 (or R5)	0	50k	87.5k	124k	212.5k	312.5k
R3 (or R6)	100k	100k	100k	100k	100k	100k

NOTE: The minimum output capacitor value is given for different output voltage to make sure the whole converter system is stable. Output capacitance should increase to support faster load transient requirement.

TABLE 3. SUMMARY OF DIFFERENCES

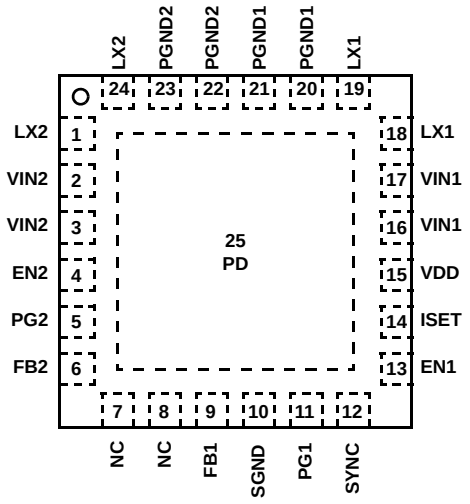
PART NUMBER	SWITCHING FREQUENCY
ISL8033	Internally fixed switching frequency F_{SW} = 1MHz
ISL8033A	Internally fixed switching frequency F_{SW} = 2.5MHz

Block Diagram



Pin Configuration

ISL8033, ISL8033A
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 24	LX2	Switching node connection for Channel 2. Connect to one terminal of inductor for VOUT2.
22, 23	PGND2	Negative supply for the power stage of Channel 2.
4	EN2	Regulator Channel 2 enable pin. Enable the output, VOUT2, when driven to high. Shutdown the VOUT2 and discharge output capacitor when driven to low. Do not leave this pin floating.
5	PG2	1ms timer output. At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the VOUT2 voltage.
6	FB2	The feedback network of the Channel 2 regulator. FB2 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB2. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB2 to monitor the Channel 2 regulator output voltage.
7, 8	NC	No connect pins. Please tie to GROUND.
9	FB1	The feedback network of the Channel 1 regulator. FB1 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB1. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB1 to monitor the Channel 1 regulator output voltage.
10	SGND	System ground. Make a single point connection from these pins to PGND.
11	PG1	1ms timer output. At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the VOUT1 voltage.
12	SYNC	Connect to logic high or input voltage VIN. Connect to an external function generator for external Synchronization. Negative edge trigger. Do not leave this pin floating. **Do not tie this pin low (or to SGND).**
13	EN1	Regulator Channel 1 enable pin. Enable the output, VOUT1, when driven to high. Shutdown the VOUT1 and discharge output capacitor when driven to low. Do not leave this pin floating.
14	ISET	ISET is the output current limit setting of the regulators. See the “” table on page 6 for settings.
15	VDD	Input supply voltage for the logic. Connect VIN pin.
20, 21	PGND1	Negative supply for the power stage of Channel 1.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
18, 19	LX1	Switching node connection for Channel 1. Connect to one terminal of inductor for VOUT1.
2, 3, 16, 17	VIN2, VIN1	Input supply voltage. Connect a 22µF ceramic capacitor to power-ground per channel.
25	PD	The exposed pad must be connected to the PGND pin for proper electrical performance. Add as much vias as possible under this pad for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8033IRZ*	80 33IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL8033AIRZ*	80 33AIRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D

NOTES:

1. Add “-T*” suffix for tape and reel.Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8033, ISL8033A. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings (Reference to SGND)

VIN1,VIN2, VDD . . . . . -0.3V to 6.5V (DC) or 7V (20ms)
LX1, LX2 . . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
EN1, EN2, PG1, PG2, SYNC, ISET . . . . . -0.3V to +6.5V
FB1, FB2 . . . . . -0.3V to 2.7V
NC . . . . . -0.3V to 0.3V
ESD Ratings
Human Body Model (Tested per JESD22-A114) 4kV
Charged Device Model (Tested per JESD22-C101E) 2kV
Machine Model (Tested per JESD22-A115) 0.3kV
Latch Up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package (Notes 4, 5)	36	2

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 2.85V to 6V
Load Current Range per Channel . . . . . 0A to 3A
Junction Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
INPUT SUPPLY						
VIN Undervoltage Lockout Threshold	V_{UVLO}	Rising		2.5	**2.85**	V
		Hysteresis	**50**	100		mV
Quiescent Supply Current						
	I_{VDD}	SYNC = VDD, EN1 = EN2 = VDD, F_S = 1MHz, no load at the output		15	**40**	mA
		SYNC = VDD, EN1 = EN2 = VDD, F_S = 2.5MHz, no load at the output		30	**70**	mA
Shutdown Supply Current	I_{SD}	VDD = 6V, EN1 = EN2 = SGND		8	**20**	µA
OUTPUT REGULATION						
FB1, FB2 Regulation Voltage	V_{FB}		**0.790**	0.8	**0.810**	V
FB1, FB2 Bias Current	I_{FB}	VFB = 0.75V		0.1		µA
Load Regulation		SYNC = VDD, output load from 0A to 3A		2		mV/A
Line Regulation		VIN = VO + 0.5V to 6V (minimal 2.85V)		0.1		%/V
Soft-Start Ramp Time Cycle				1.5		ms
COMPENSATION						
Error Amplifier Trans-Conductance				20		µA/V
Trans-Resistance	RT		**0.18**	0.2	**0.22**	Ω
OVERCURRENT PROTECTION						
Dynamic Current Limit ON-time	t_{OCON}			17		Clock pulses
Dynamic Current Limit OFF-time	t_{OCOFF}			8		SS cycle

Electrical Specifications Unless otherwise noted, the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN1 = EN2 = VDD, L = 1.5µH, C1 = C2 = C4 = 2x22µF, I_{OUT1} = I_{OUT2} = 0A to 3A. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Positive Peak Overcurrent Limit	I_{poc1}	ISET = VDD	**4.1**	4.8	**5.5**	A
	I_{poc2}		**4.1**	4.8	**5.5**	A
	I_{poc1}	ISET = Float	**4.1**	4.8	**5.5**	A
	I_{poc2}		**2.7**	3.3	**3.9**	A
	I_{poc1}	ISET = GND	**2.7**	3.3	**3.9**	A
	I_{poc2}		**2.7**	3.3	**3.9**	A
Negative Peak Overcurrent Limit	I_{noc1}		**-3.5**	-2.5	**-1.5**	A
	I_{noc2}		**-3.5**	-2.5	**-1.5**	A
LX1, LX2						
P-Channel MOSFET ON-Resistance		VIN = 6V, I_O = 200mA		50	**75**	mΩ
		VIN = 2.85V, I_O = 200mA		70	**100**	mΩ
N-Channel MOSFET ON-Resistance		VIN = 6V, I_O = 200mA		50	**75**	mΩ
		VIN = 2.85V, I_O = 200mA		70	**100**	mΩ
LX_ Maximum Duty Cycle				100		%
PWM Switching Frequency	F_S	ISL8033	**0.88**	1.1	**1.32**	MHz
		ISL8033A	**2.15**	2.5	**2.85**	MHz
Synchronization Range	F_{SYNC}	ISL8033 (Note 6)	**2.64**		**6**	MHz
Channel 1 to Channel 2 Phase Shift		Rising edge to rising edge timing		180		°
LX Minimum On-Time		SYNC = High (forced PWM mode)			**140**	ns
Soft Discharge Resistance	R_{DIS}	EN = LOW	**80**	100	**120**	Ω
LX Leakage Current		Pulled up to 6V		0.1	**1**	µA
PG1, PG2						
Output Low Voltage		Sinking 1mA, VFB = 0.7V			**0.3**	V
PG_ Pin Leakage Current		PG = VIN = 6V		0.01	**0.1**	µA
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	**89.5**	92	**94.5**	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	**85**	88	**91**	%
Delay Time (Rising Edge)				1		ms
Internal PGOOD Delay Time (Falling Edge)				7	**10**	µs
EN1, EN2, SYNC						
Logic Input Low					**0.4**	V
Logic Input High			**1.5**			V
SYNC Logic Input Leakage Current	I_{SYNC}	Pulled up to 6V		0.1	**1**	µA
Enable Logic Input Leakage Current	I_{EN}	Pulled up to 6V		0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. The operational frequency per switching channel will be half of the SYNC frequency.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Operating Performance ISL8033

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = L2 = 1.5µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A.

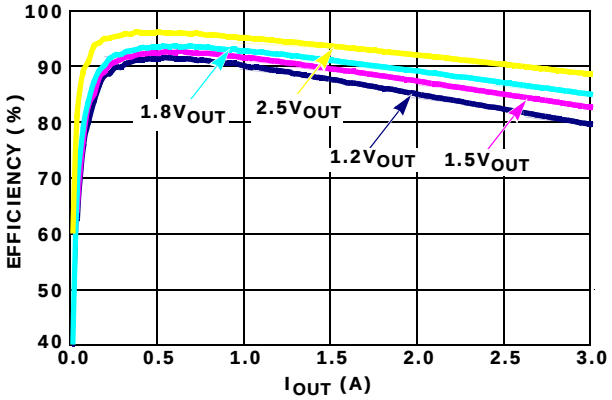


FIGURE 3. EFFICIENCY, T_A = +25°C V_{IN} = 3.3V

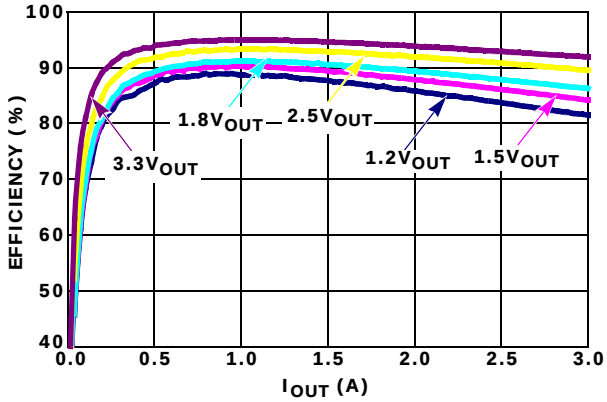


FIGURE 4. EFFICIENCY, T_A = +25°C, V_{IN} = 5V

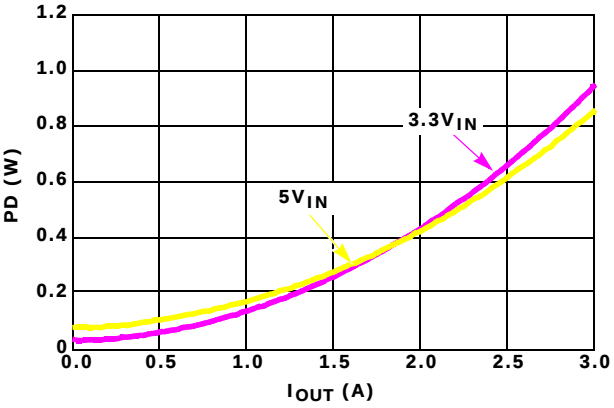


FIGURE 5. POWER DISSIPATION, T_A = +25°C V_{OUT} = 1.8V

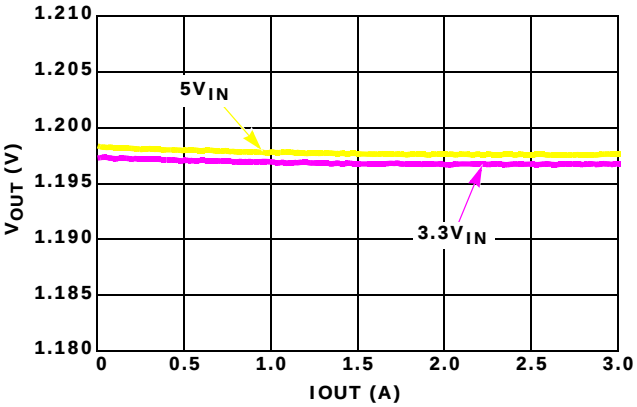


FIGURE 6. LOAD REGULATION, V_{OUT} = 1.2V T_A = +25°C

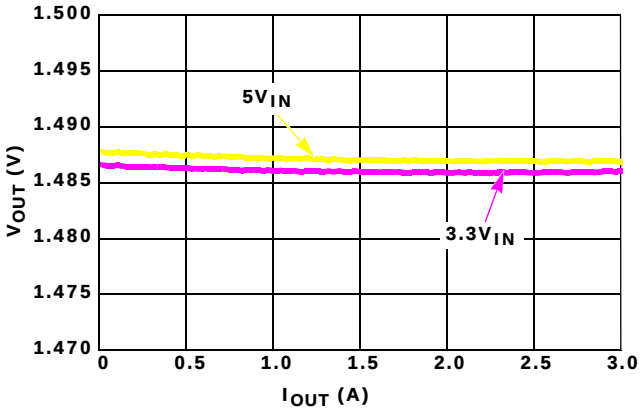


FIGURE 7. LOAD REGULATION, V_{OUT} = 1.5V T_A = +25°C

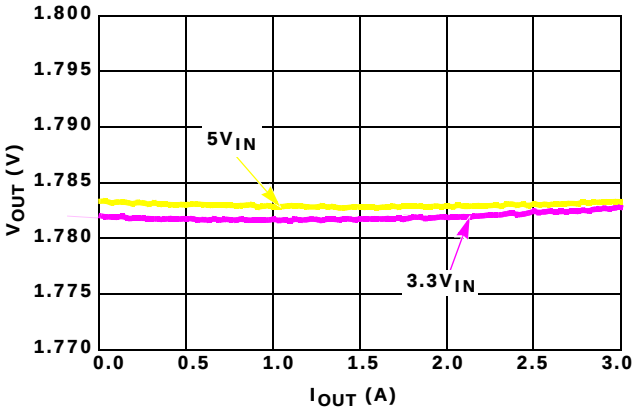


FIGURE 8. LOAD REGULATION, V_{OUT} = 1.8V T_A = +25°C

Typical Operating Performance ISL8033

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = L2 = 1.5µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A. **(Continued)**

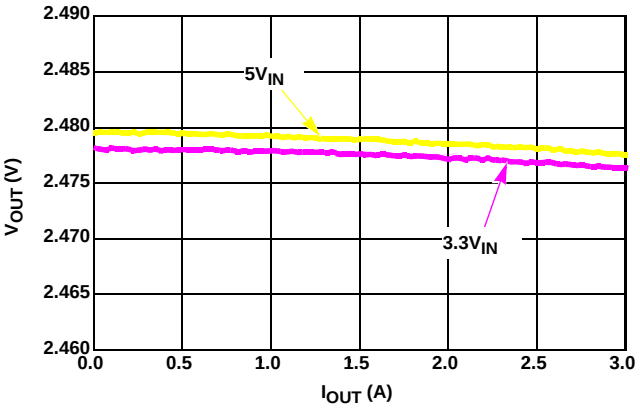


FIGURE 9. LOAD REGULATION, V_{OUT} = 2.5V T_A = +25°C

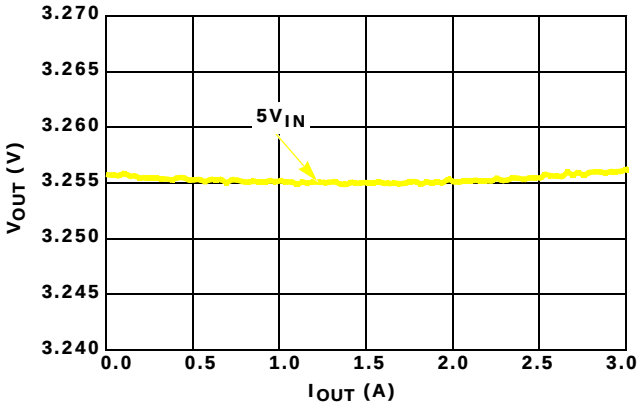


FIGURE 10. LOAD REGULATION, V_{OUT} = 3.3V T_A = +25°C

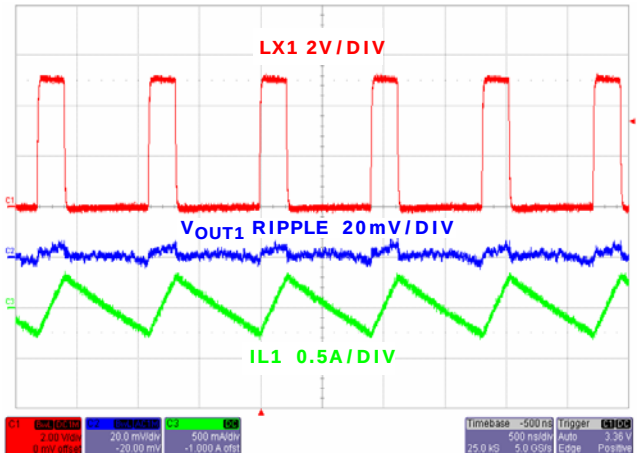


FIGURE 11. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 (PWM)

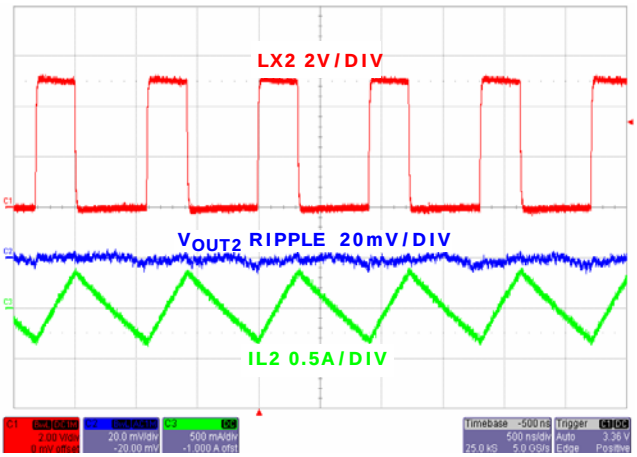


FIGURE 12. STEADY STATE OPERATION AT NO LOAD CHANNEL 2 (PWM)

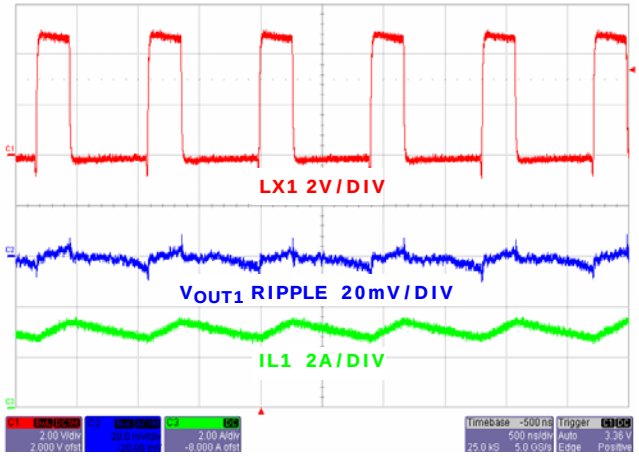


FIGURE 13. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

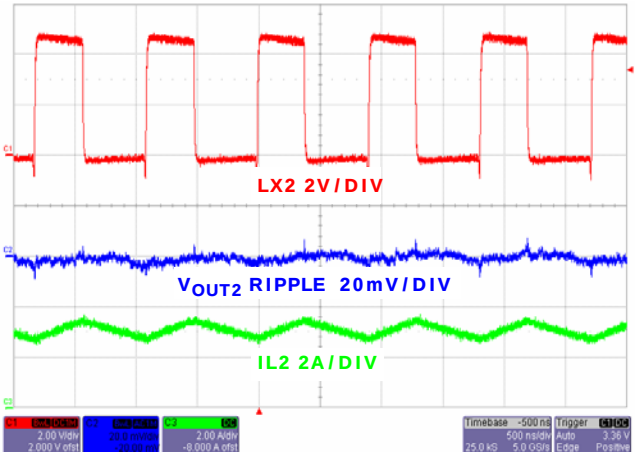


FIGURE 14. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

Typical Operating Performance ISL8033

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = L2 = 1.5µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A. **(Continued)**

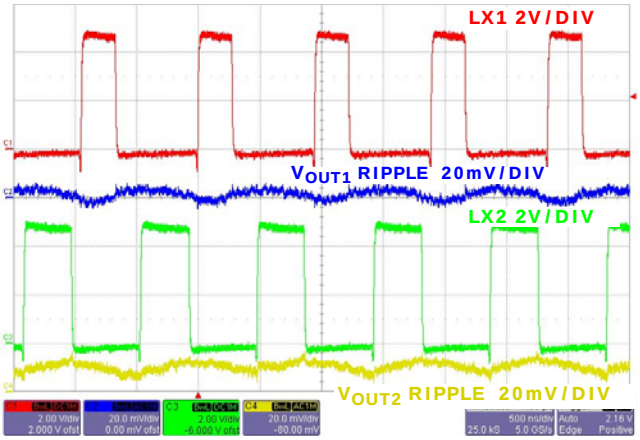


FIGURE 15. STEADY STATE OPERATION WITH FULL LOADS AT BOTH CHANNELS

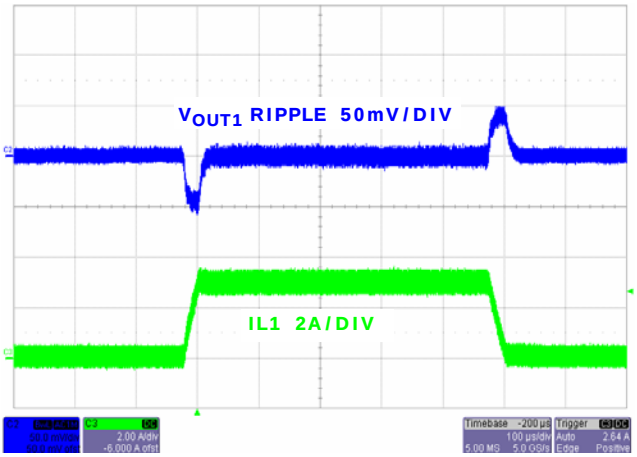


FIGURE 16. LOAD TRANSIENT CHANNEL 1 (PWM)

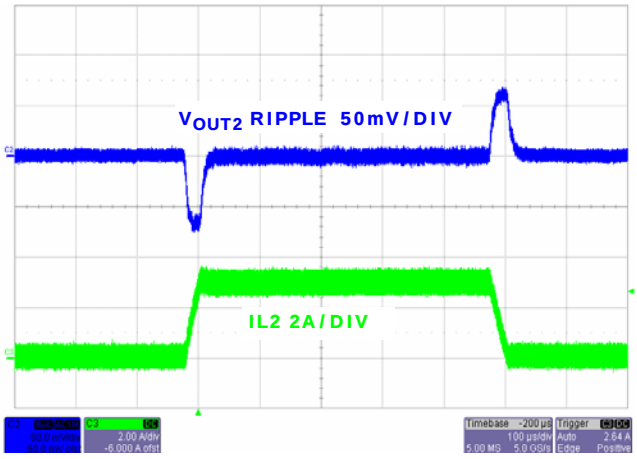


FIGURE 17. LOAD TRANSIENT CHANNEL 2 (PWM)

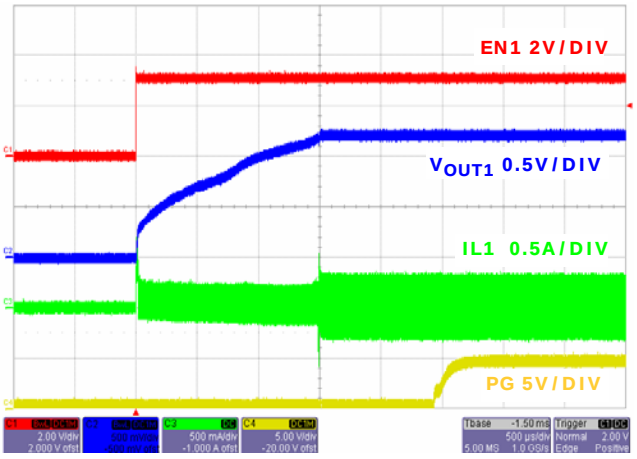


FIGURE 18. SOFT-START WITH NO LOAD CHANNEL 1

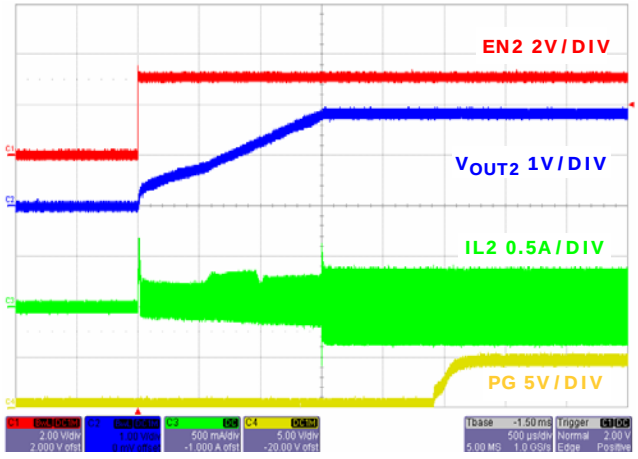


FIGURE 19. SOFT-START WITH NO LOAD CHANNEL 2

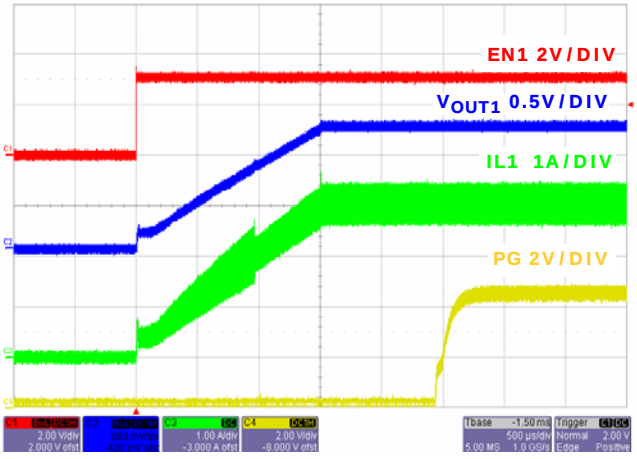


FIGURE 20. SOFT-START AT FULL LOAD CHANNEL 1

Typical Operating Performance ISL8033

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = L2 = 1.5µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A. **(Continued)**

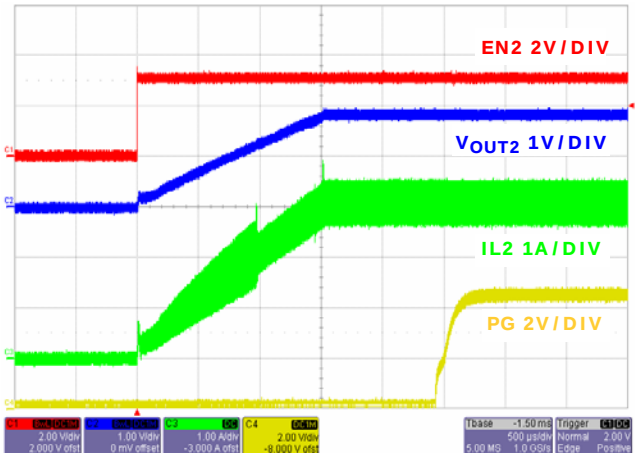


FIGURE 21. SOFT-START AT FULL LOAD CHANNEL 2

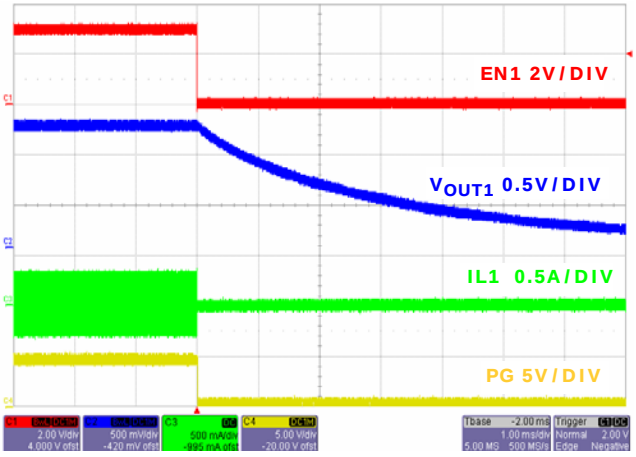


FIGURE 22. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

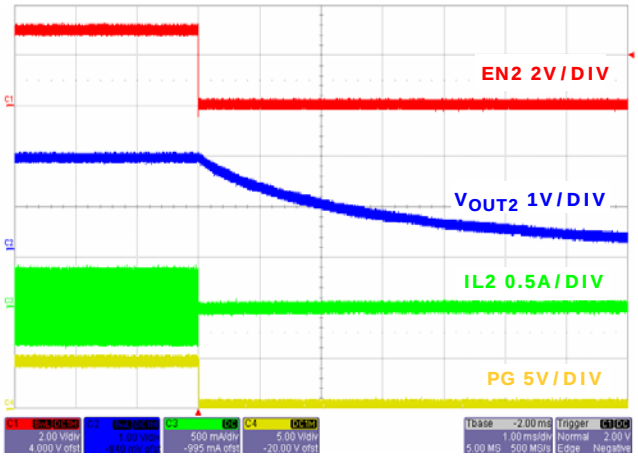


FIGURE 23. SOFT-DISCHARGE SHUTDOWN CHANNEL 2

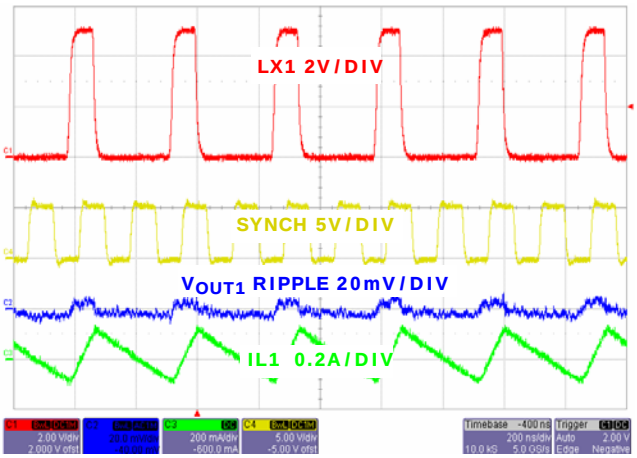


FIGURE 24. CHANNEL 1 STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 6MHz

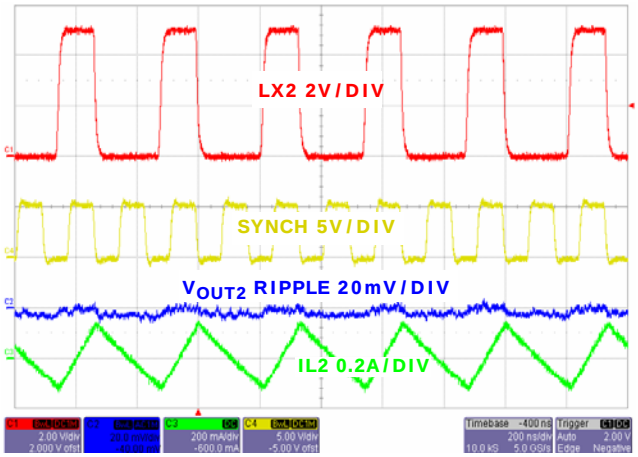


FIGURE 25. CHANNEL 2 STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 6MHz

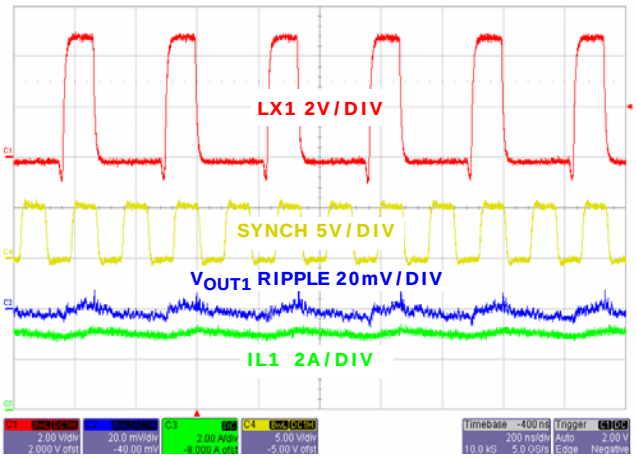


FIGURE 26. CHANNEL 1 STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 6MHz

Typical Operating Performance ISL8033

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = L2 = 1.5µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A. **(Continued)**

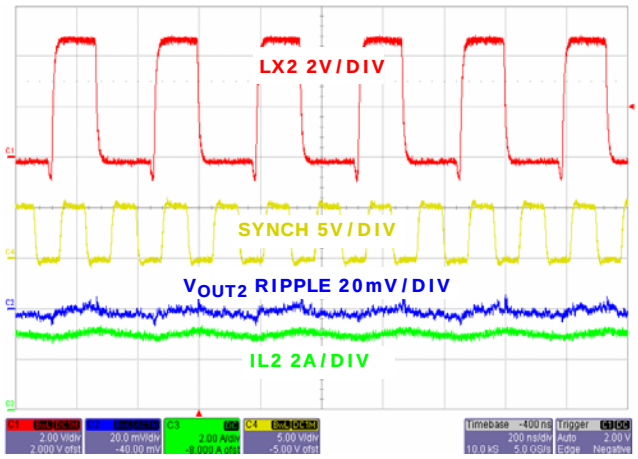


FIGURE 27. CHANNEL 2 STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 6MHz

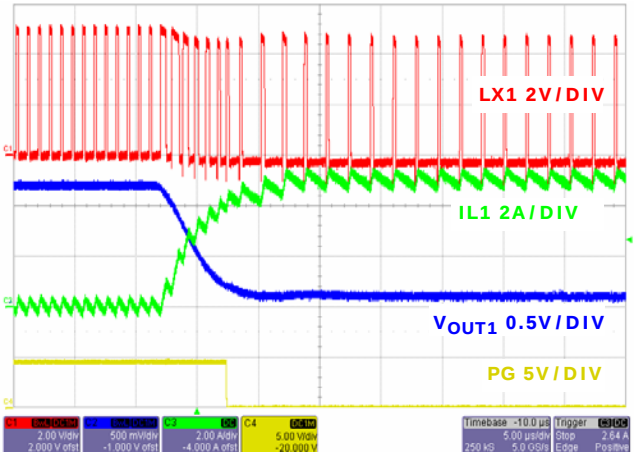


FIGURE 28. OUTPUT SHORT CIRCUIT CHANNEL 1

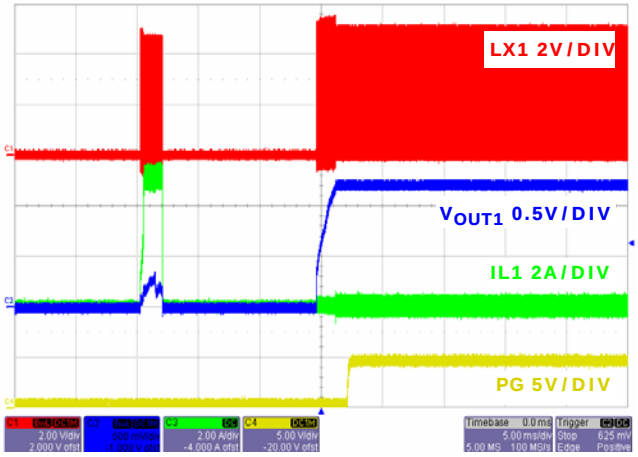


FIGURE 29. OUTPUT SHORT CIRCUIT RECOVERY CHANNEL 1

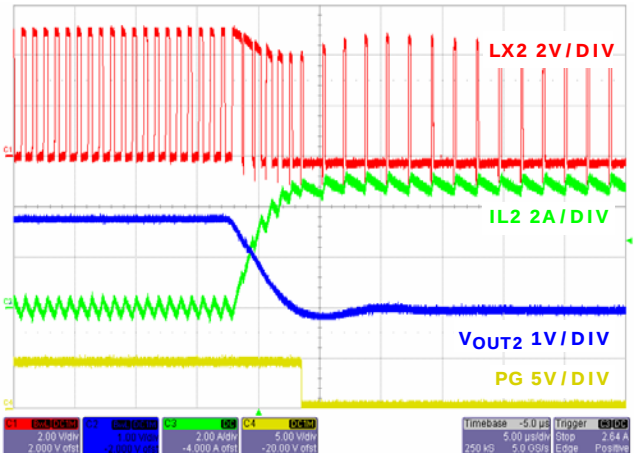


FIGURE 30. OUTPUT SHORT CIRCUIT CHANNEL 2

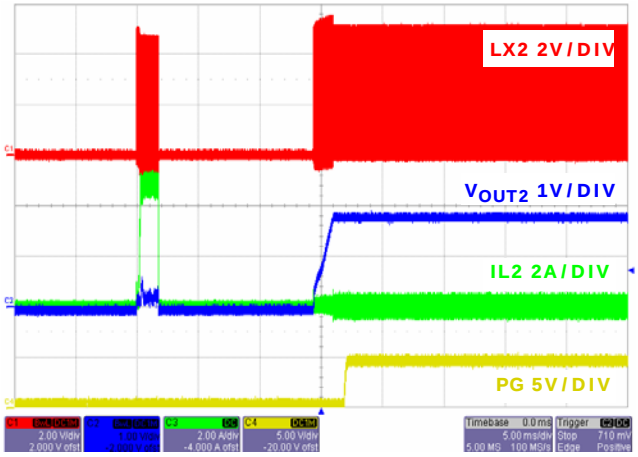


FIGURE 31. OUTPUT SHORT CIRCUIT RECOVERY CHANNEL 2

Typical Operating Performance ISL8033A

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = 0.68µH, L2 = 1µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A.

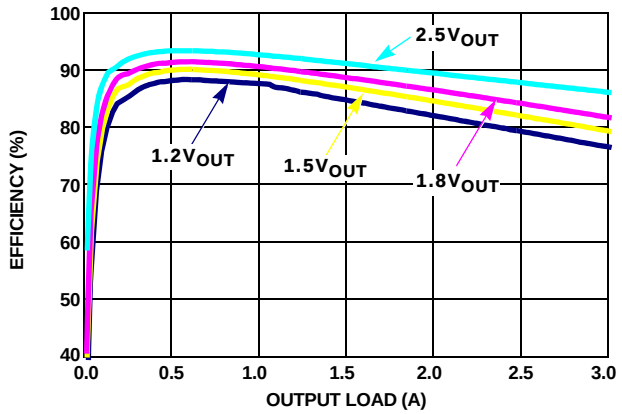


FIGURE 32. EFFICIENCY vs LOAD, 1MHz 3.3V_{IN} DUAL CH1 +25°C

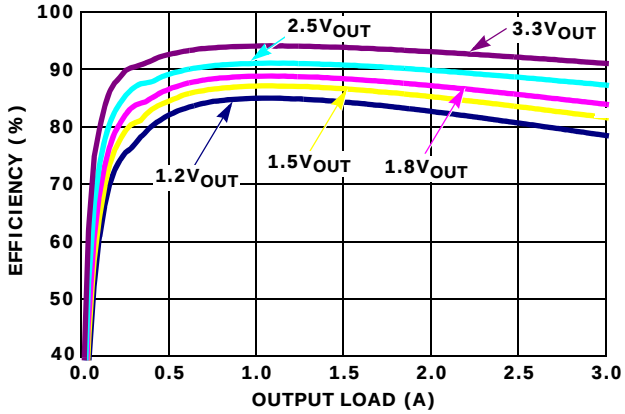


FIGURE 33. EFFICIENCY vs LOAD, 1MHz 5V_{IN}, DUAL CH1 +25°C

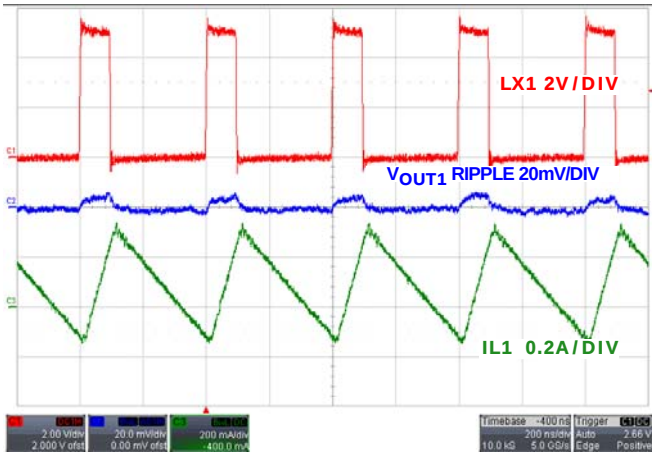


FIGURE 34. STEADY STATE OPERATION AT NO LOAD CHANNEL 1

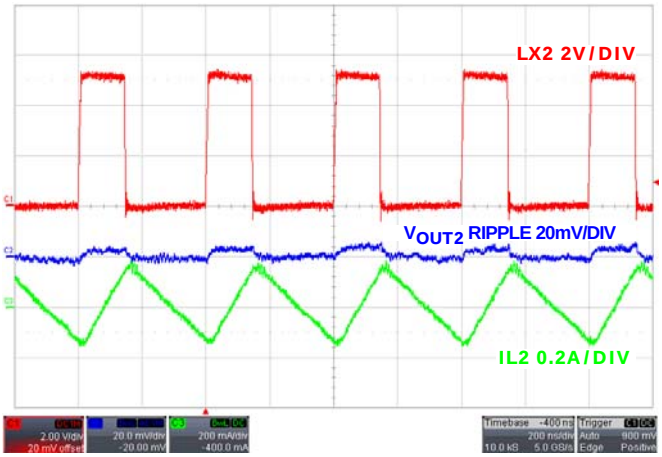


FIGURE 35. STEADY STATE OPERATION AT NO LOAD CHANNEL 2

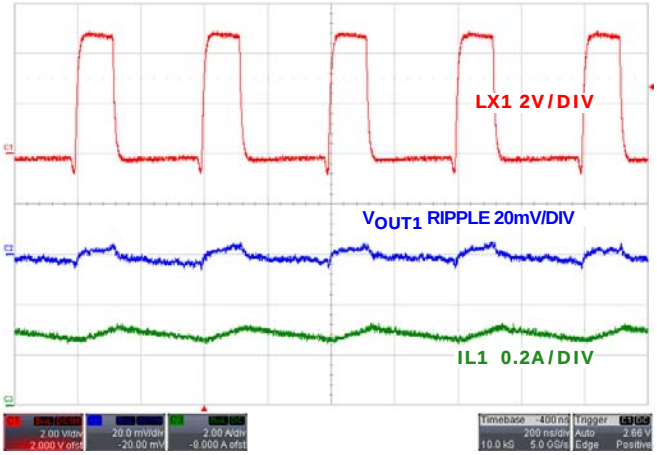


FIGURE 36. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 1

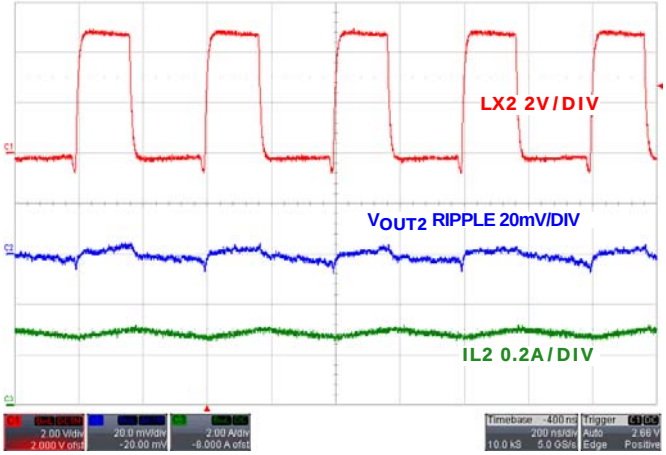


FIGURE 37. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

Typical Operating Performance ISL8033A

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 5V, EN = V_{IN}, L1 = 0.68µH, L2 = 1µH, C1 = C2 = C4 = 2x22µF, V_{OUT1} = 1.2V, V_{OUT2} = 1.8V, I_{OUT1} = I_{OUT2} = 0A to 3A. **(Continued)**

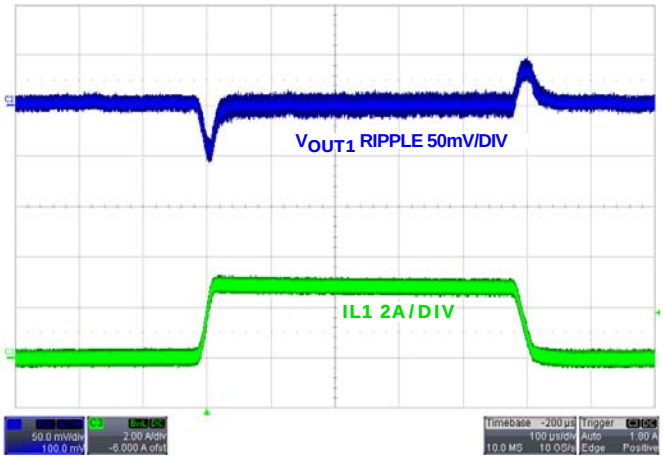


FIGURE 38. LOAD TRANSIENT CHANNEL 1

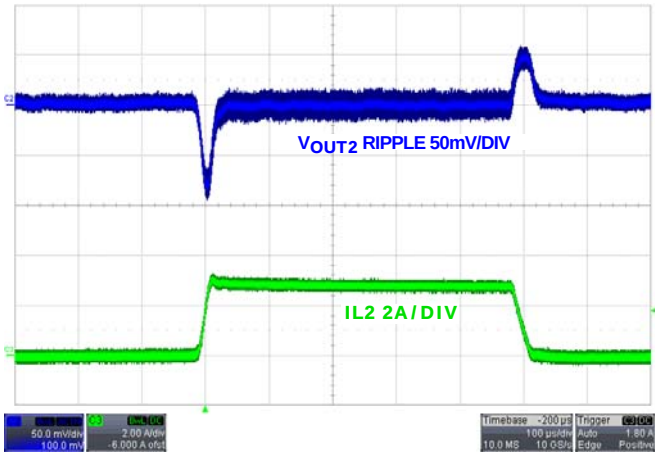


FIGURE 39. LOAD TRANSIENT CHANNEL 2

Theory of Operation

The ISL8033 is a dual 3A step-down switching regulator optimized for battery-powered or mobile applications. The regulator operates at 1MHz fixed switching frequency under heavy load condition. The ISL8033A operates at 2.5MHz to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. The two channels are 180° out-of-phase operation. The supply current is typically only 8µA when the regulator is shutdown.

PWM Control Scheme

Pulling the SYNC pin HI (>1.5V) forces the converter into PWM mode in the next switching cycle regardless of output current. Each of the channels of the ISL8033, ISL8033A employ the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting, as shown in the "Theory of Operation" on page 14. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-channel MOSFET when it is turned on and the current sense amplifier CSA1. The gain for the current sensing circuit is typically 0.20V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier CSA1 (or CSA2 on Channel 2) and the compensation slope (0.46V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 40 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA_ output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 390kΩ RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

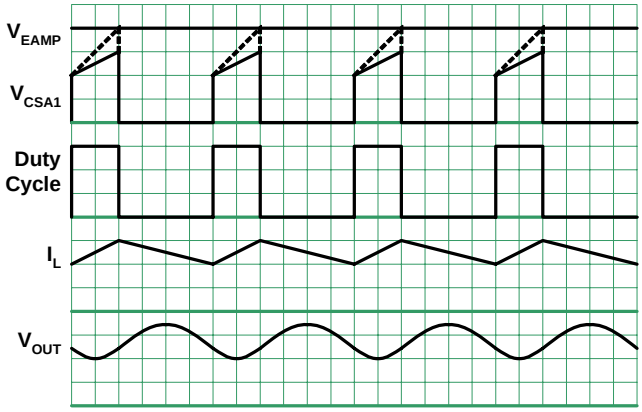


FIGURE 40. PWM OPERATION WAVEFORMS

Synchronization Control (ISL8033)

The frequency of operation can be synchronized up to 6MHz by an external signal applied to the SYNC pin. The 1st falling edge on the SYNC triggered the rising edge of the PWM ON pulse of Channel 1. The 2nd falling edge of the SYNC triggers the rising edge of the PWM ON pulse of the Channel 2. This process alternates indefinitely allowing 180° output phase operation between the two channels.

Overcurrent Protection

CAS1 and CSA2 are used to monitor Output 1 and Output 2 channels respectively. The overcurrent protection is realized by monitoring the CSA output with the OCP threshold logic, as shown in Figure 40. The current sensing circuit has a gain of 0.20V/A, from the P-MOSFET current to the CSA output. When the CSA1 output reaches the threshold set by ISET, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the Overcurrent Fault Counter is set to 1 and the Overcurrent Condition Flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC Fault Counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shutdown under an Overcurrent Fault Condition. An Overcurrent Fault Condition will result in the regulator attempting to restart in a hiccup mode with the delay between restarts being 4 soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC Fault Counter reaching a count of four, the Overcurrent Condition Flag will set back to LOW.

If the negative output current reaches -2.5A, the part enters Negative Overcurrent Protection. At this point, all switching stops and the part enters tri-state mode while the pull-down FET is discharging the output until it reaches normal regulation voltage, then the IC restarts.

PG

There are two independent power-good signals. PG1 monitors the Output Channel 1 and PG2 monitors the Output Channel 2. When powering up, the open-collector Power-On Reset output holds low for about 1ms after V_O reaches the preset voltage. The PG_ output also serves as a 1ms delayed Power-Good signal.

UVLO

When the input voltage is below the undervoltage lock out (UVLO) threshold, the regulator is disabled.

Enable

The enable (EN) input allows the user to control the turning on or off the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft-start-up will begin.

Soft Start-Up

The soft start-up eliminates the inrush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising 1/2 speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.5V; hence the PWM operating frequency is 1/2 of the normal frequency.

When the IC ramps up at start-up, it can't sink current even at PWM mode.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, or the output undervoltage fault latch is set, its output discharges to PGND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimize for best efficiency. The ON-resistance for the P-MOSFET is typically 50mΩ and the ON-resistance for the N-MOSFET is typical 50mΩ.

100% Duty Cycle

The ISL8033 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8033, ISL8033A can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum drop-out voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL8033, ISL8033A has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shutdown. As the temperature drops to +125°C, the ISL8033, ISL8033A resumes operation by stepping through a soft start-up.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operation, ISL8033 typically uses a 1.5µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for a higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

The inductor's saturation current rating needs be at least larger than the peak current. The ISL8033, ISL8033A protects the typical peak current 4.8A. The saturation current needs be over 4.8A for maximum output current application.

ISL8033, ISL8033A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values for the ISL8033, ISL8033A are shown in Tables 1 and 2 on page 2.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider, which is used to scale the output voltage

relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 2.

The output voltage programming resistor, R_2 (or R_5 in Channel 2), will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 0Ω and 750kΩ. Let R_2 = 124kΩ, then R_3 will be:

$$R_3 = \frac{R_2 \times 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 2)}$$

For better performance, add 12pF in parallel to R_2. If the output voltage desired is 0.8V, then leave R_3 unpopulated and short R_2.

Input Capacitor Selection

The main functions for the input capacitor is to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. One 22µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection per channel.

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL8033, the power loop is composed of the output inductor L's, the output capacitor C_{OUT1} and C_{OUT2}, the LX's pins, and the SGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the LX_ pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as closely as possible to the VIN pin . Also, the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
1/12/2011	FN6854.2	Throughout: Converted to new datasheet template P1: Added “Related Literature” P5: Updated Tape & Reel note in “Ordering Information” from "Add “-T” suffix for tape and reel." to new standard "Add “-T*” suffix for tape and reel." The "*" covers all possible tape and reel options P6: Updated over temp note in Min Max column of spec tables from "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to new standard "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."
10/12/10	FN6854.1	In Table 3 on page 2, corrected F_{SW} for ISL8033 from 1Hz to 1MHz
9/29/10	FN6854.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL8033, ISL8033A

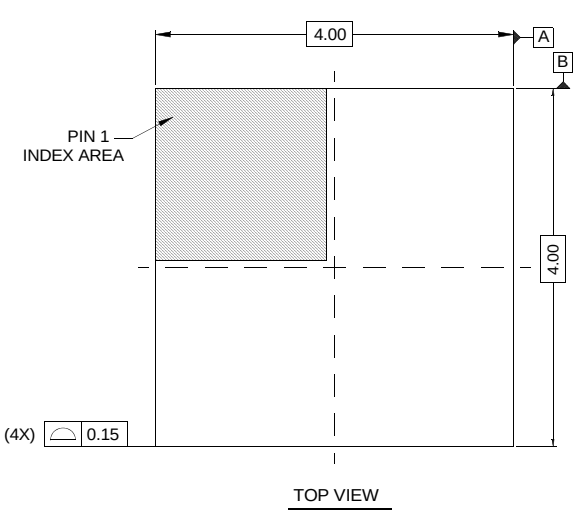
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

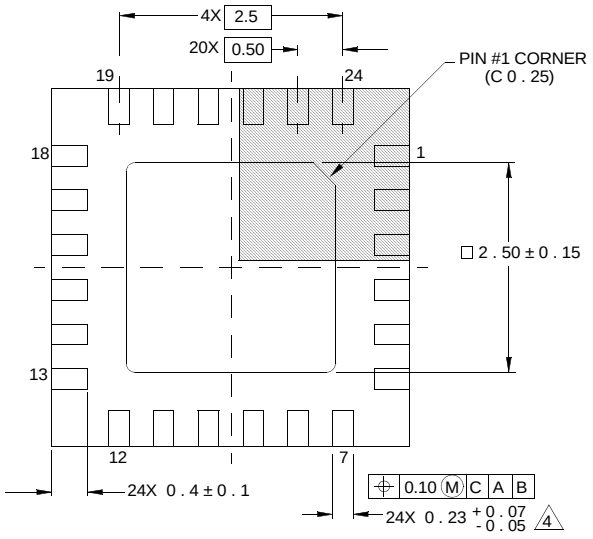
Package Outline Drawing

L24.4x4D

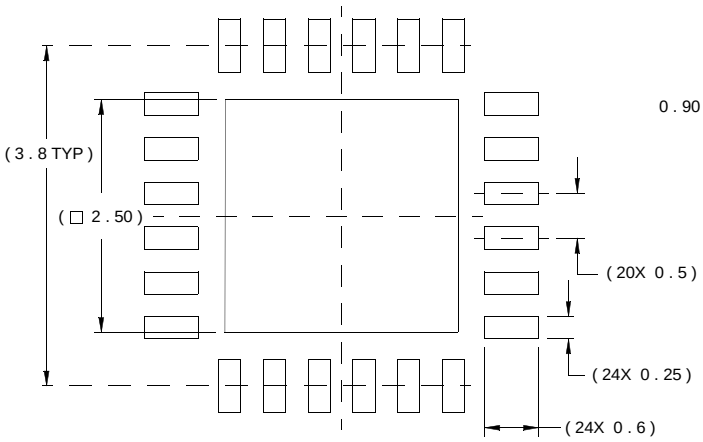
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



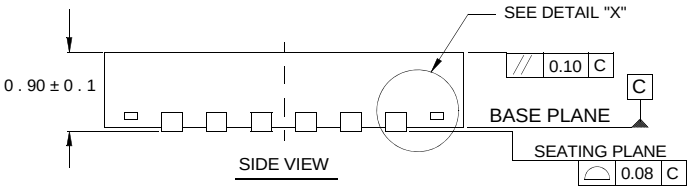
TOP VIEW



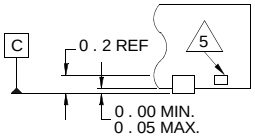
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.